

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.116

Serial Number: 10/674,835

Filing Date: September 29, 2003

Title: BRANCH-AWARE FIFO FOR INTERPROCESSOR DATA SHARING

Assignee: Intel Corporation

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Dkt: 42P17022

REMARKS

This responds to the Office Action mailed on December 19, 2006.

Claims 14, 20, 33, 37, 48, 50, and 58 are amended herein.

Claim Objections

Claims 20-22 were objected to as being dependent on a rejected base claim, but were identified as being allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. On page 9, paragraph 12, the Final Office Action recites that the arguments regarding claims 20-22 have been considered and found persuasive. Therefore, these claims have been rewritten as suggested and are now in condition for allowance.

Additionally, the patentably distinguishing elements from claim 20 have been copied into independent claims 37, 48, 50, and 58, which should make these claims and those that depend therefrom similarly patentable.

35 USC § 101 Rejection of the Claims

Claims 14-22, 33, 35, 37 and 48-76 were rejected under 35 USC §101 because the claimed invention is deemed to be directed to non-statutory subject matter. The Office Action applies an improper test to these claims. The proper test involves determining whether a claim produces a useful, concrete, tangible, real-world result. Here, the results are repeatable, determinable, capable of being detected, and produce a physical transformation of at least a pop pointer in a FIFO memory. The Office Action asserts that this physical transformation is not a tangible result since it is only a manipulation of data in a computer. This is incorrect.

This type of analysis and rejection is typically applied to the processing of numbers and formulae that are not displayed or stored or used to control a process. Here, the physical transformation is used to control retrieval of and writes of a pointer value to a FIFO memory. Thus, the tangible result includes not only physically transforming the pop pointer of the FIFO memory but also controlling the contents of a FIFO memory and thus controlling how future reads occur. This control has been added to amended claim 14. Thus, not only are bits rearranged, but the useful, concrete, tangible result of controlling a FIFO memory is explicitly called out.

Claim 33 describes a processing unit that can perform speculative execution. The processing unit includes several elements. The Office Action asserts that there is no practical application because “no output is generated and outputted.” This is incorrect.

There are two output FIFO memories. The first output FIFO memory is “to output data from the processing unit.” The second output FIFO memory is to “drive output data from the processing unit.” Clearly the processing unit is producing outputs. These outputs are used to control a process. A system that controls an internal process of a machine produces a concrete, tangible, real-world result even though that result may only be experienced inside the computer. The “output” from the system may be provided to another internal element of the computer.

Consider a system that controls the position of a read/write head on a disk drive. No examiner would argue that there is no practical application because if they opened up the system they could see the read/write head move back and forth as data is read/written from the disk. Here, there is analogous control of accesses to solid state memory rather than to a spinning platter. The read/write “head” still needs to be positioned. Thus, the Office Action is incorrect
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when it asserts that the processing unit produces no output. Additionally, the output satisfies the practical utility test since it controls a process. Therefore the 101 rejection is improper and should be removed.

The Office Action asserts that claim 37 generates and produces no output. However, claim 37 reads, in line 15-16: “a first output FIFO memory coupled to a last processor of the plurality of processors **to drive output data** from the multiprocessor.” Claim 37 also reads, in line 36-37: “a second output FIFO memory coupled to the first of the plurality of processors **to drive output data** from the multiprocessor.”

Clearly the Office Action is incorrect when it asserts that “no output is generated and outputted.” Not only is output generated and output, it is used to control a process. Therefore the 101 rejection is improper and should be removed.

The Office Action asserts that claim 48 fails to provide a tangible result since no output is provided. This is incorrect. Claim 48 reads, in line 4-5: “**to pass data** from the processor to another processor.” Claim 48 also reads, in line 19-20: “a second branch-aware FIFO memory **to pass data** from another processor to the processor.” Clearly an output is being generated. Claim 48 has been amended to describe the use of the data.

The Office Action asserts that claim 50 does not produce a tangible result because it only retrieves a pointer value. This is incorrect. Claim 50 includes a control logic “**to control retrieving** a pointer value ... based ... on program branching information.” Producing an output that controls whether a pointer is retrieved is clearly statutory subject matter because it produces a useful, concrete, tangible, real-world result.

35 USC § 112 Rejection of the Claims

Claim 18 was rejected under 35 USC §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. The Office Action asserts that there is insufficient antecedent basis for the term “the memory array”. This is incorrect. The antecedent appears in claim 17, line 3 “storing data into a memory array...”

Claim 37 was rejected under 35 USC §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. The Office Action asserts that there is insufficient antecedent basis for the term “the processing unit” in line 15. Claim 37 has been amended to change the term to “multi-processor” and therefore resolve the antecedent basis problem.

35 USC § 103 Rejection of the Claims

Claims 14-17 and 23-25 were rejected under 35 USC §103(a) as being unpatentable over Buckenmaier (U.S. Patent 5,388,074) in view of Crouse et al. (U.S. Patent 4,831,517). Claim 14 has been amended in a manner that renders claim 14 patentable, which similarly renders claims 14-19 similarly patentable. Claims 23-25 were previously cancelled and thus their rejection is irrelevant.

Claims 50 and 52-53 were rejected under 35 USC §103(a) as being unpatentable over O'Connor et al. (US Patent 6,532,531) in view of Crouse et al. (U.S. Patent 4,831,517). The patentable elements of claim 20 have been copied into claim 50, rendering claims 50-57 similarly patentable.

Claims 51 and 54-56 were rejected under 35 USC §103(a) as being unpatentable over O'Connor (US Patent 6,532,531) and Crouse et al. (U.S. Patent 4,831,517) and further in view of Buckenmaier (U.S. Patent 5,388,074). The patentable elements of claim 20 have been copied into claim 50, rendering claims 50-57 similarly patentable.

Claim 57 was rejected under 35 USC §103(a) as being unpatentable over O'Connor (US Patent 6,532,531) and Crouse et al. (U.S. Patent 4,831,517) and further in view of Dally et al. (U.S. Patent Publication 2003/0070059). The patentable elements of claim 20 have been copied into claim 50, rendering claims 50-57 similarly patentable.

Claims 58-60, 63, 64, 67-69 and 72-74 were rejected under 35 USC §103(a) as being unpatentable over Daniel et al. (US Patent Publication 2001/0047439) in view of Dally et al. (U.S. Patent Publication 2003/0070059). The patentable elements of claim 20 have been copied into claim 58, rendering claims 58-66 similarly patentable.

Claims 61, 62, 65, 66, 70, 71, 75 and 76 were rejected under 35 USC §103(a) as being unpatentable over Daniel et al. (US Patent Publication 2001/0047439) in view of Dally et al. (U.S. Patent Publication 2003/0070059) and further in view of Crouse (US Patent 4,831,517)

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Conclusion

Applicant respectfully submits that the amended claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney ((216) 348-5844) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 13-0265.

Respectfully submitted,

JOSE S. NIELL ET AL.

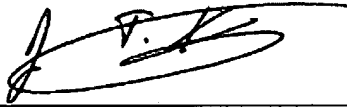
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Date March 15, 2007

By



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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 15 day of March, 2007.

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